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FLOW-GATING I

by

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1. The Gating Problem

A simple problem occurring in a computer is to transfer a zero or a one from one place to another in a selective fashion. The problem may be presented by discussing the transmission of information from one Eccles-Jordan flipflop to another. It will be assumed that non-overlapping voltage bands represent the zero and one signals, the bands being caused by parameter drift. An Eccles-Jordan flipflop, then, has the following abstract properties (see figure 1):

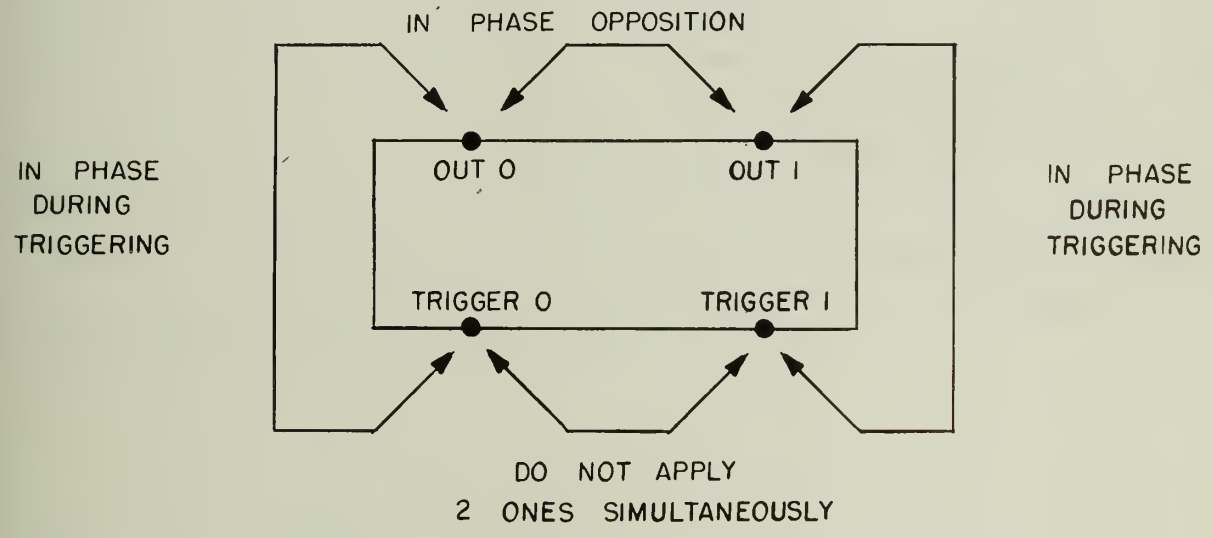


Figure 1
ABSTRACT REPRESENTATION OF AN ECCLES-JORDAN FLIPFLOP

There are two low impedance outputs and two high impedance trigger points. Points with the same number are in phase; points with a different number are out of phase. (In general, -- especially in so-called last-moving-point flipflops -- there may be a time lag between a trigger point and the corresponding "in phase output".) OUT 0

in the one state corresponds to the zero state of the flipflop. OUT 1 in the one state coresponds to the one state of the flipflop. Transmission of information between two flipflops can be accomplished by connecting the outputs of the first to the inputs of the second by means of switches. The direction of flow of information wil be determined by the asymmetry of the impedances; the lower impedance drives the higher impedance. This does not mean that the voltages in the connecting wires lie necessarily in the zero or one bands while the flipflops are tied together. It does mean, however, that once the switches are opened, flipflop 1 has copied the state of flipflop 2 independently of the order in which the switches were opened.

The important point to note is that a gate in the form of two switches severs the connections which transmit information, thus allowing the triggered circuit to seek its levels inside the permitted bands. This severing action can be achieved by adding two diodes in front of trigger point 0 and trigger point 1. In figure 2 the situation is indicated for the case of positive logic (one signal voltages greater than zero signal voltages). If the point marked IN are kept at the zero level, the trigger points are effectively disconnected, except perhaps for some small currents due to the difference in the applied zero voltage and the natural zero voltage of a trigger point. In order to allow the trigger points to seek their own level, the two inputs can be held at the most negative zero voltage. This will be termed a floating output of the diodes.

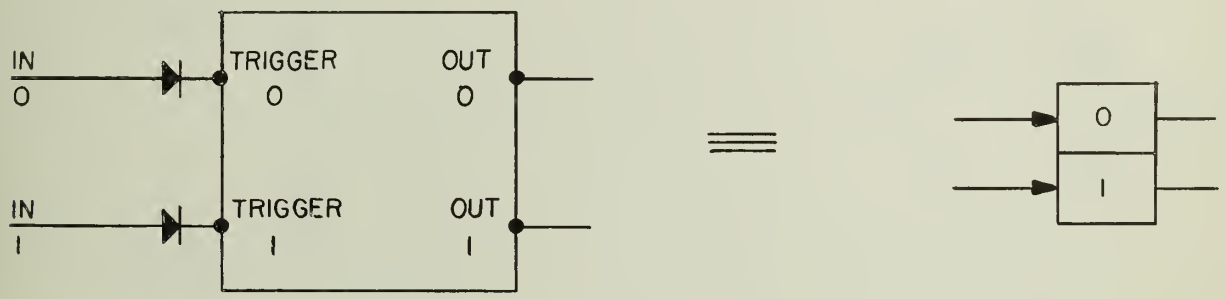


Figure 2
MAKE-UP OF AN ECCLES-JORDAN FLIPFLOP

Note that one can also pull the trigger points down by using diodes in the opposite direction. Then, the floating output would be caused by the most positive one voltage. The discussion will, however, be limited to the first case.

Transmitting information between two Eccles-Jordan flipflops with input diodes now only necessitates the use of two AND circuits with a sufficiently low output impedance. To inhibit the flow of information, a zero signal is injected into the second inputs of the AND's. This double-gating system can be simplified by setting the first flipflop to the standard zero state by an initial clearing signal which is turned off before a single AND (connected between the one sides) receives the gating one signal which causes the conditional transfer. This clearing and gating is naturally slower than double gating since it essentially involves two distinct operations. It should be noted that in both these gating systems the trigger point is either left as it is (floating or zero input) or pushed up.

In flipflops of the non-symmetric variety, like a Schmitt trigger (operationally equivalent to an Eccles-Jordan with only two in-phase points accessible!), the double-gating problem is somewhat harder to solve. This can be seen in figure 3. A single trigger point has to be pushed up (to gate a one), or to be pulled down (to gate a zero) or finally to be disconnected from the incoming signal in order for the device to stay in its last state.

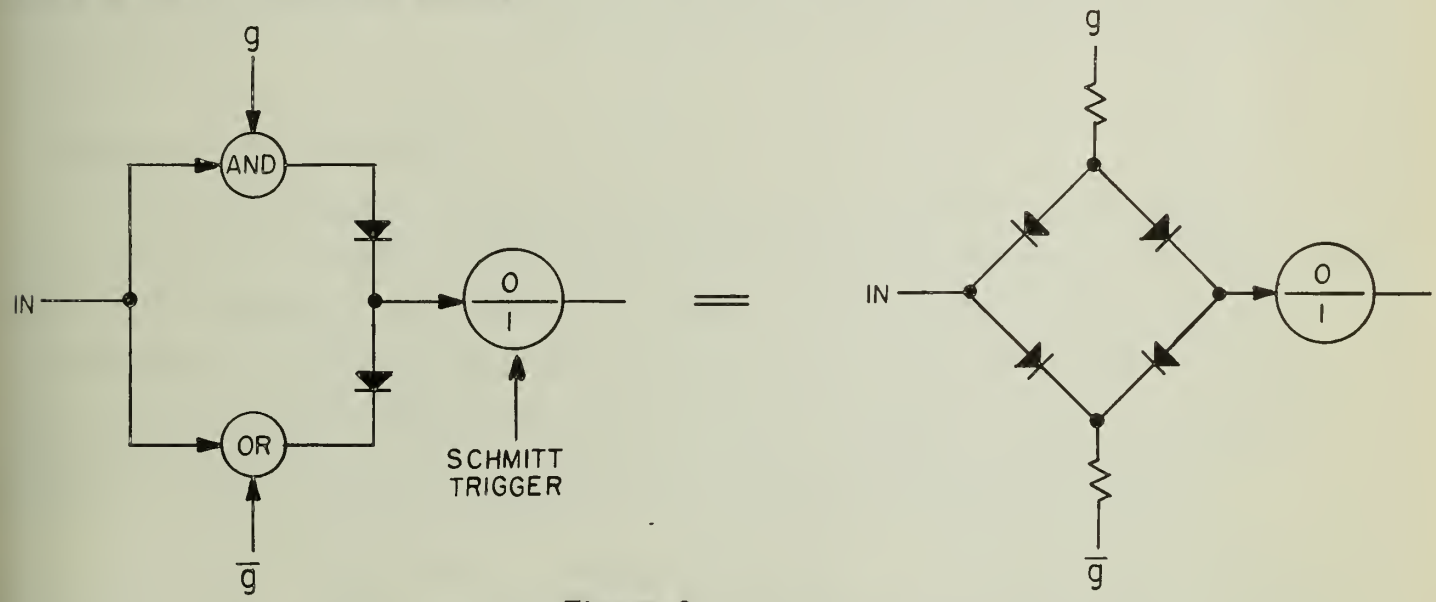


Figure 3

DOUBLE GATING A SCHMITT TRIGGER

A single diode is only able to transmit information in one direction, therefore, it is evident that going into the trigger point two diodes must be used. It turns out that one of the paths then necessitates an OR gate and a second input which is the complement of the gating signal. Furthermore, inspection shows that there is no essential difference (even topologically) between the latter arrangement and a bridge modulator type of gate as indicated in the right-hand side of figure 3.

Although g and $\bar{g}$ do not have to be in exact phase opposition, the production of push-pull gating signals is rather cumbersome, especially when control applications -- with only a small number of flipflops connected to any given gating bus -- are considered. The bridge modulator gating system can, and has been, used for registers. Here, the fact that two gates can be connected "upside-down" can be used to provide mutually exclusive paths.

The gating problem for the Schmitt trigger type of flipflop is, of course, quite easily solved in case clearing precedes the gating. One AND circuit and one diode are sufficient to set the circuit to the one state once it has been cleared to zero. The only objection to this method is, again, its comparatively slower speed since gating-in again involves two operations. The next section describes a gating system which is essentially a clearing and gating system, but in which the two operations occur simultaneously. Furthermore, no special clearing signal has to be provided from the outside.

2. The Flow-Gating Principle

The main idea in flow-gating is to vary the potentials of two flipflops in such a way that "transfer diodes" connected between the flip-flops are conditionally conducting (depending on the state of the sending flipflop) when these potentials are made unequal. In the normal (equal) potential condition the "transfer diodes" are cut off and produce the severing action discussed in the last section. The word "flow-gating" has been chosen to characterize these systems, in which information flows up or down a potential gradient established between bistable elements.

It will be shown that the idea can be applied to bistable elements of a very general class. Take any dc-bistable circuit having two trigger points P and Q such that a sufficiently positive voltage applied to P triggers it into the zero

state while a sufficiently positive voltage applied to Q produces the one state. Also suppose that there is a (low impedance) output S in phase with Q (the out-of-phase output could be discussed too). It is not necessary, or even desirable, that the voltage swings at P, Q and S be the same. It will even be assumed that (under all tolerance conditions) Q and P have non-overlapping swings. Suppose, more specifically, that the voltages q and s at points Q and S have the property that -- (1) and (0) designating the flipflop state --

$$q(1) > q(0) > s(1) > s(0) \quad . \tag{1}$$

Consider the supply voltages of the circuit. Rename potentials in such a way that the lowest supply voltage is called ground, and obtain all other voltages from dividers between this new ground and the highest supply voltage E. This will not change the operation of the circuit. In particular, the circuit is still going to be bistable, and the three points of interest, P, Q and S, will each exhibit two voltages p(1), p(0), q(1), q(0) and s(1), s(0) depending on the state. In each one of the states, however, all voltages are going to be proportional to E because of the dc stability assumption. In other words,

$$\begin{aligned} p(1) &= p_1 E & p(0) &= p_o E \\ q(1) &= q_1 E & q(0) &= q_o E \\ s(1) &= s_1 E & s(0) &= s_o E \end{aligned} \tag{2}$$

where $p_1 p_o$ ... etc. are constants. (1) now simply becomes

$$q_1 > q_o > s_1 > s_o \quad . \tag{3}$$

Under slightly idealized circumstances (negligible hysteresis, etc.), the critical trigger voltages to be applied to P and Q to trigger either a zero or a one are

$$\frac{p_o + p_1}{2} E = pE \quad \text{(say)}$$

$$\frac{q_o + q_1}{2} E = qE \quad \text{(say)} \qquad (4)$$

To simplify the discussion, it will also be assumed that the output impedance is very low, i.e., s_o and s_1, will be assumed independent of the load.

Now, connect two flipflops fitting the above description as in figure 4, i.e., connect Q_1 and S_2 through a "transfer diode" D_1, and connect P_1 through a diode D_o to a fixed potential u_o. The value of u_o will be determined later. It is evident in view of (3) that flipflop 1 and flipflop 2 are quite independent as long as their supply voltages are the same. D_1 will not be conducting for any combination of states. This corresponds to what was called a "floating output" in the preceding section.

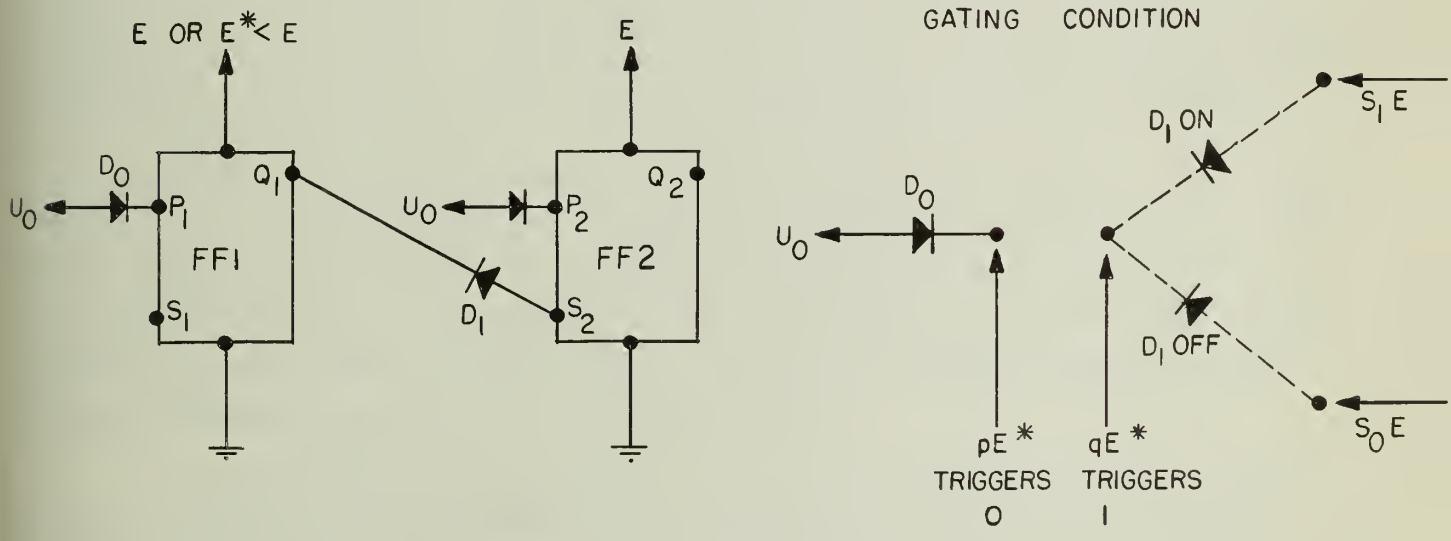


Figure 4

THE FLOW-GATING PRINCIPLE

(vertical distances indicate potential above ground)

To gate information from flipflop 2 to flipflop 1, E is lowered to a value E^*, such that the arithmetic mean of the two possible potentials of S (for E) becomes equal to the trigger potential of Q (for E^*). E^* is given by

$$qE^* = \frac{s_1 + s_o}{2} E \quad . \tag{5}$$

Furthermore, u_o is chosen to be slightly bigger than the trigger potential of P (for E), i.e.,

$$u_o > pE^* = \frac{p}{q} \frac{s_1 + s_o}{2} E \quad . \tag{6}$$

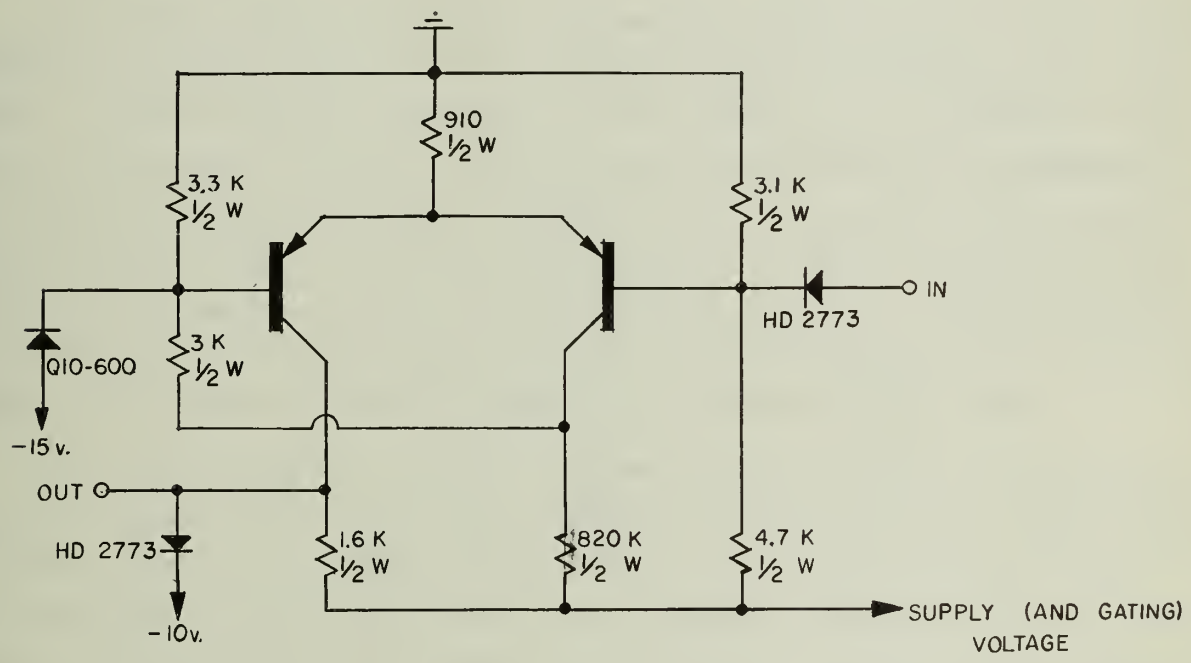
It is easily seen that (3), (4), (5) and (6) (together with the connections of figure 4) guarantee a complete transfer of information between the flipflops, for if flipflop 2 is in the one state, $s_1 E > qE^*$ and D_1 conducts, thus setting flipflop 1 to the one state. If, however, flipflop 2 is in the zero state ($s_o E < qE^*$), diode D_1 is ineffective (although it may conduct slightly), and diode D_o is going to set flipflop 1 to the zero state. There may, of course, arise the question, "Why is setting through D_1 possible while D_o counteracts?" The answer is that it is always possible to arrange for $s_1 E$ to override u_o by providing a large enough swing at the output.

Once the information has been received, the supply voltage is made to rise back to E; the state impressed is "trapped" in the process. That the circuit really cannot change its state as the E^* to E change occurs can be seen as follows. If a zero has been stored, D_1 is off and D_o is on (see figure 4). As the supply voltage increases, Q and P become more positive. D_1 certainly cannot be turned on again. A similar argument holds when a one has been stored.

It is now clear why flow-gating is a sort of clearing and gating system in which both the clearing operation and the AND-gate function are performed by modifying the potential of the whole circuit. Practically, this means that a fairly large current and a large voltage swing have to be provided by the gate drivers. If it is desired to obtain easier driver conditions, in particular, if the gate-in signal has to be furnished by a flow-gating flipflop, a separate driver transistor can be added, having the flipflop between its collector and ground and a load resistor of appropriate size.

3. Practical Example of a Flow-Gating Flipflop and Its Use

Consider the circuit of figure 5, giving what is probably the simplest flow-gating flipflop, i.e. a modified Schmitt trigger. The trigger points P and Q are the bases of the two transistors, and the output S is the collector of the "emitter follower" T_1. Taking the output from this point does not impair the left-hand transistor's function in the flipflop. Note that S is in phase with Q as was assumed in the last section. There is, however, one slight difference. For practical purposes pnp transistors were used, and this necessitates changing the sign of all potentials with respect to ground. E becomes -E, u_o becomes $-u_o$, etc. The general theory is, of course, still valid after this change.



MAXIMUM INPUT CURRENT: 2.75 mA.

MINIMUM OUTPUT CURRENT: 3.75 mA.

OUTPUT VOLTAGES: -10v. AND -20v. (NOMINAL)

SUPPLY AND GATING VOLTAGE: -20v. (NORMAL)

-45v. (GATE-IN)

OPERATION TIME: < 50 mμs.

Figure 5

LAYOUT OF A FLOW-GATING FLIPFLOP

The circuit values are chosen in such a way that under the worst drift conditions, i.e., a 2% drift of resistor values, a 3% drift of voltage supplies and a transistor α anywhere between .98 and 1.00 (which means using selected GF-45011 transistors), the circuit still works satisfactorily. In order to verify this, the exact circuit equations and inequalities were analyzed by Illiac, the electronic computer at the University of Illinois. The base-emitter drops were stored in table form for fixed values of the emitter current, and linear interpolation was used to obtain intermediate values. The analysis was preceded by an optimizing process in which all equations were linearized in the neighborhood of a given set of parameters. After several steps, a near optimum solution was obtained and used as the basis for the analysis programs.

The figure gives all pertinent information, like input and output currents and output and supply voltages. A few indications about the "setting time" might be useful. The most reliable characteristic of a circuit is its "operation time", obtained by connecting in series n similar circuits and measuring the propagation time of a given state from one end to the other (e.g., by connecting the circuits in cascade and observing the resultant oscillation). A similar procedure is hard to realize for flow-gating, and it is more realistic actually to swing the supply voltages up and down for each gating operation. One way of doing this is indicated in figure 6 which shows the use of flow-gating in a binary counter stage.

The counter works as follows: Suppose that when we have a one (positive logic) at the input to the first driver, flipflops (1) and (3) are in their "normal", more positive, state, i.e., that they cannot receive information. Due to the NOT circuit, flipflops (2) and (4) are then in the "gating", more negative, state, and information will be gated from (1) into (4) and from (3) into (2). When IN now goes back to a zero, the contents of (2) and (4) will be sent to (1) and (3), respectively. If we put into the four flipflops the initial pattern 0011, we shall observe cyclic shifting. Looking at one of the flipflops (OUT), we see square pulses, the period of which is twice that of the incoming symmetric square wave, i.e., we have a frequency divider. Of course, the device is asynchronous if alternate non-overlapping gating signals are provided by the two drivers.

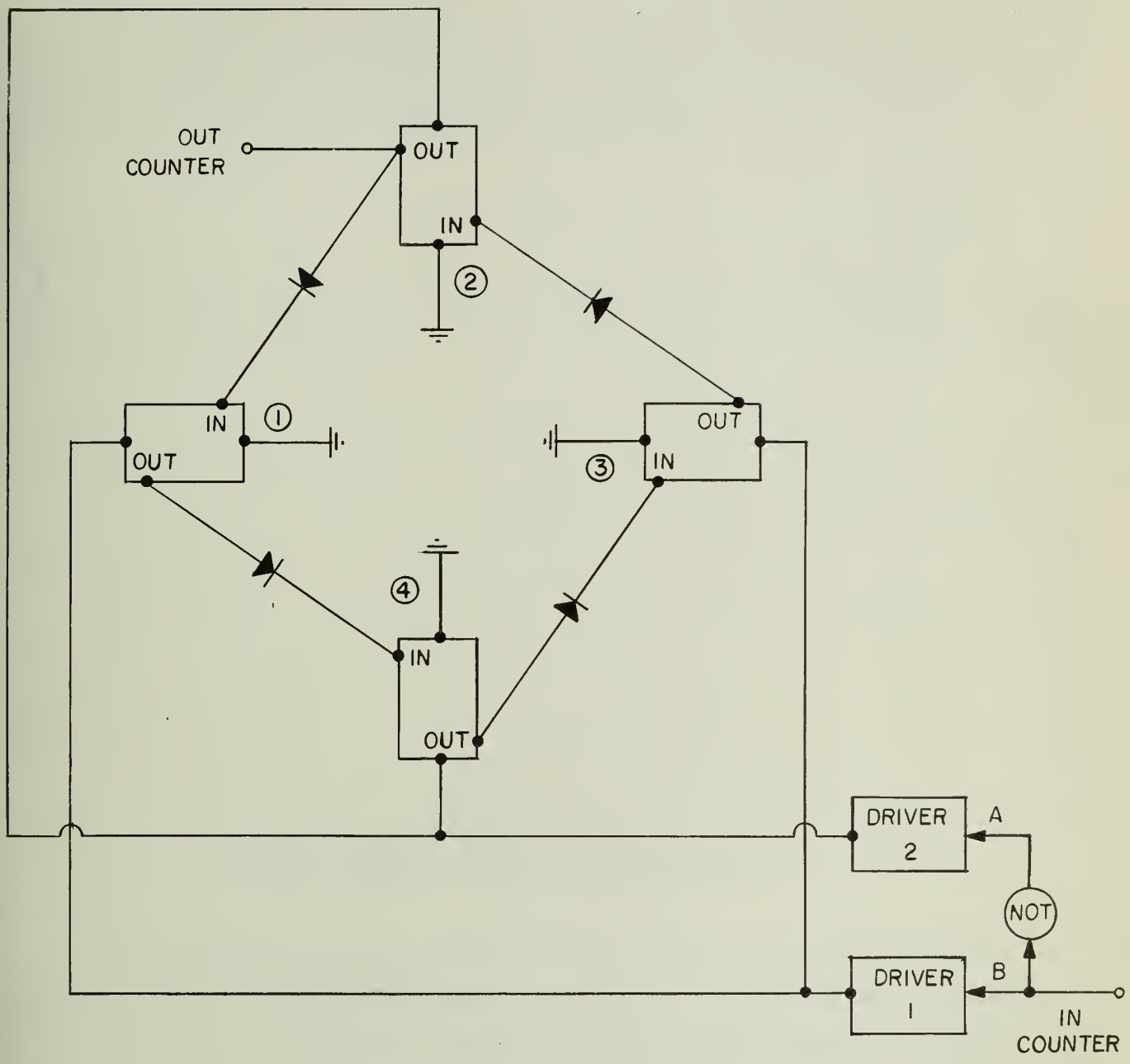


Figure 6

A FLOW-GATING BINARY COUNTER STAGE

Figure 7 shows the output of a flipflop when the input is a 5 mc sinewave. Satisfactory operation can be obtained at nearly twice that frequency. This shows that the setting time of a flipflop is less than 50 mμs. Note that the normal output levels, i.e., -10V and -20V are overswung during the gating-in of the zero state. This does not interfere with the transmission of information to another stage since it simply cuts off the transfer diode by a greater margin.

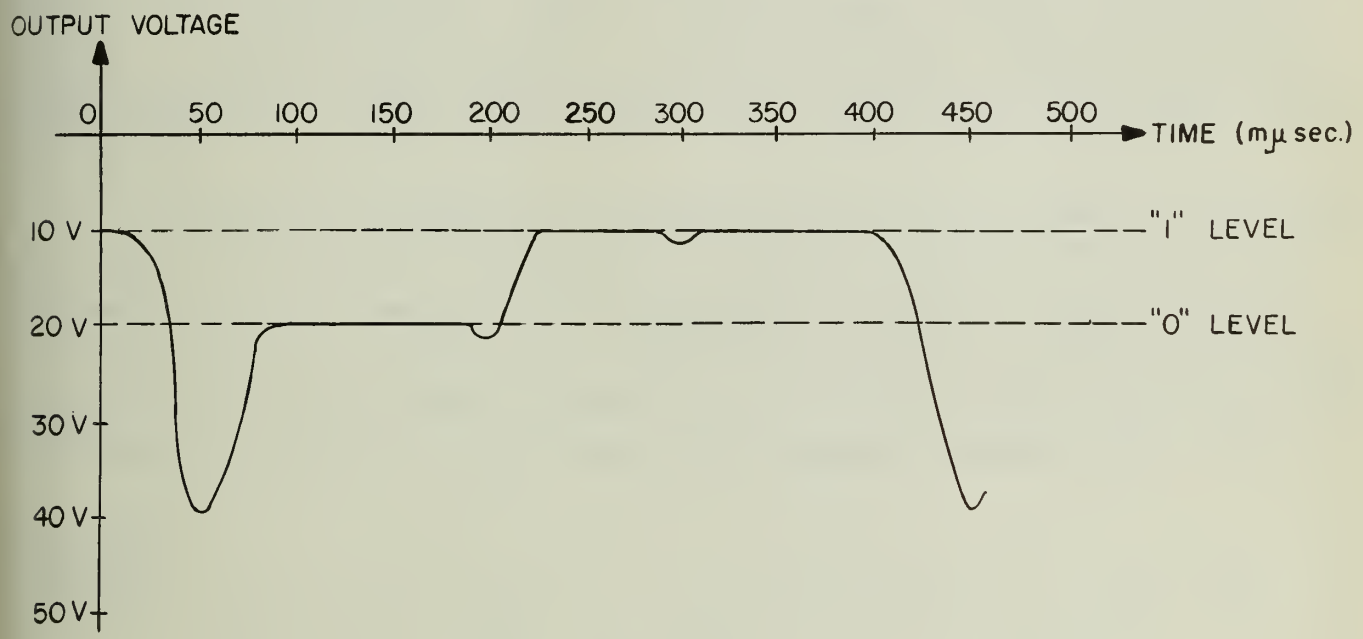


Figure 7

OUTPUT OF A FLOW-GATING FLIPFLOP IN A BINARY COUNTER. INPUT: 5 mc SINE-WAVE

It is interesting to count the number of elements involved in figure 6 to the left of points A and B. This part coresponds to a "true-toggle-false-toggle" type of counter with its associated 4 gating AND's and 2 decoding AND's commonly used in asynchronous computers. Defining complexity by C = number of transistors + 1/2 number of diodes, we obtain typically

C classical system = 25 - 31

C flow-gating = 16

4. Combination of Flow-Gating with Collector-Gating

Consider the Schmitt trigger of figure 5, and suppose that R_6 is returned to a separate voltage -T. It is then evident that as long as -T is kept negative enough, no information can be transmitted out of the flipflop even if the receiving flipflop is in its (negative) gating state: the transfer diode can never conduct. This means that the outputs of n flow-gating flipflops can be tied to a common output bus and that this bus will carry the information of that one of the flipflops which has -T in the "sending range". Here the collector-supply voltage of the emitter-follower is therefore used to provide the "gate-out" signal. This will be called collector-gating. It should be noted that this is typically a gating method on the sending side.

Similarly, the inputs of n flipflops can be tied to a common input bus and only that one which has its -E made negative enough to "gate-in" will receive the information present on the bus. This flow-gating is typically a gating method on the receiving side. The common-input-bus and common-output-bus scheme is particularly attractive for a buffer memory connected between a slow core memory and a fast arithmetic unit of a computer. Figure 8 shows the arrangement schematically.

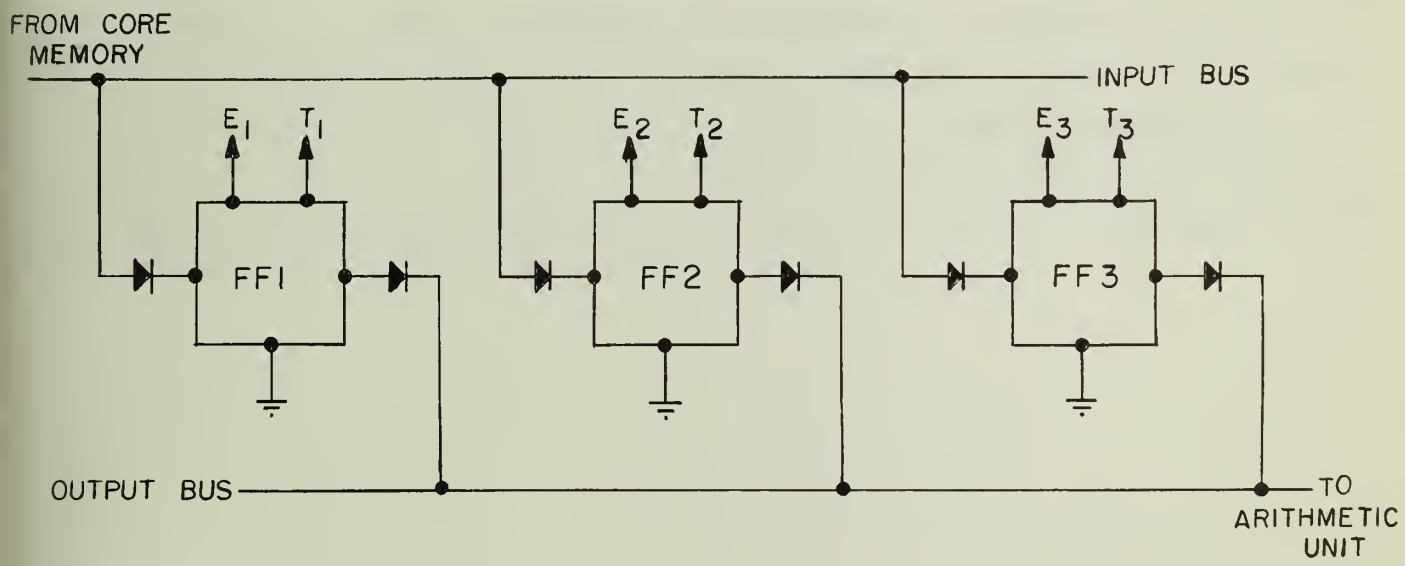


Figure 8

A FLOW-GATING BUFFER REGISTER MEMORY

The idea discussed in the last paragraph can be extended. All inputs and all outputs of n flipflops can be tied to a common bus. To transfer information from flipflop i to flipflop k, -T of flipflop i is raised, and -E of flipflop k is lowered. The two "partially selected flipflops" then have the same relative potentials as those described in section 2, i.e., the transfer diode can set the receiving flip-flop.

5. Flow-Gating Applied to Double-Gating

It is clear that flow-gating principles can be extended to include double-gating. The automatic clearing feature can then be dropped. This may not be very interesting as long as the simple transfer between two flipflops is considered, but the possibility of using partial selection (described in section 4) is quite attractive. To this end output emitter-followers are added to a classical Eccles-Jordan and their collectors are tied (through an appropriate load) to a variable supply voltage. This voltage is then raised for the sending flipflop. The receiving flipflop has the voltage supply of the cross-coupled inverters lowered until the bases of the inverters come into the "receiving region" where the two transfer diodes going into these points can (conditionally) conduct.

Finally, it should be mentioned that under some circumstances the condition of a single supply voltage for the bistable circuit can be dropped. All that is really needed is that all supply voltages E_1 E_2 ... be simultaneously reduced or increased to kE_1, kE_2 ..., k being some numerical constant. The fact that this simultaneous variation is practically quite difficult to achieve, reduces the multiple supply voltage scheme to one of only academic interest.

Acknowledgements

I wish to thank Messrs. Sylvian Ray and Neil Wiseman for their collaboration on calculations and experiments. They will summarize their work in a sequel to this report.